
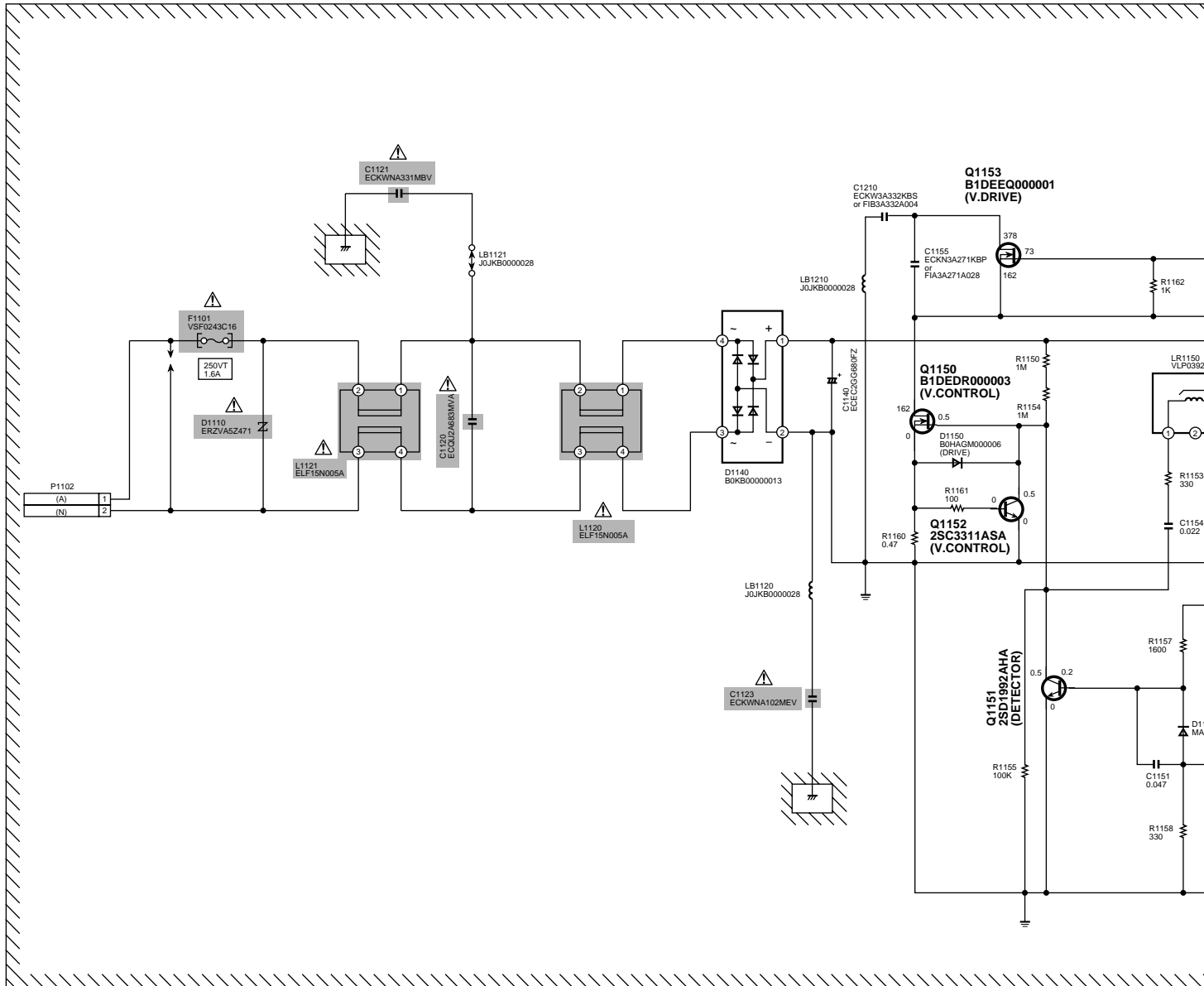


⑤ : TO SYSTEM CONTROL & SERVO / TIMER SECTION

CAUTION



THE  MARK INDICATES THE PRIMARY CIRCUIT TO DISTINGUISH THE PRIMARY FROM THE SECONDARY CIRCUIT. PAY ATTENTION NOT TO RECEIVE AN ELECTRIC SHOCK DURING REPAIR AND SERVICE OF THE PRODUCTS.

HOT



IMPORTANT SAFETY NOTICE:
COMPONENTS IDENTIFIED WITH THE MARK  HAVE THE SPECIAL CHARACTERISTICS FOR SAFETY. WHEN REPLACING ANY OF THESE COMPONENTS USE ONLY THE SAME TYPE.

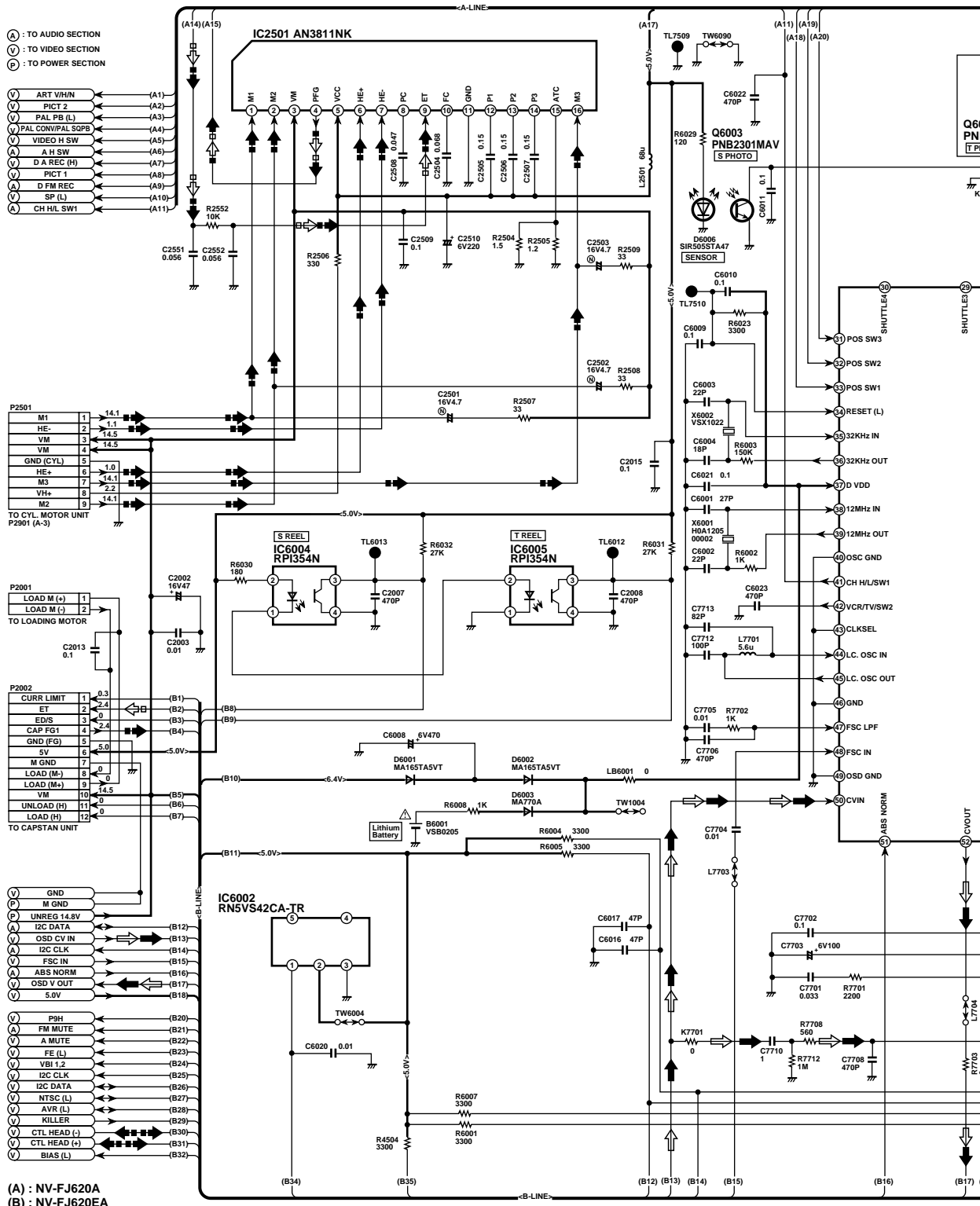
NOTE : THE MEASUREMENT MODE OF THE DC VOLTAGE ON THIS DIAGRAM IS STOP MODE.

NOTE1: WHEN MEASURE THE VOLTAGE OR WAVEFORM ON THE POWER TRANSFORMER CIRCUIT, SET THE GND TERMINAL OF MEASURING POINT AS FOLLOWS. PRIMARY SIDE...  SECONDARY SIDE... 

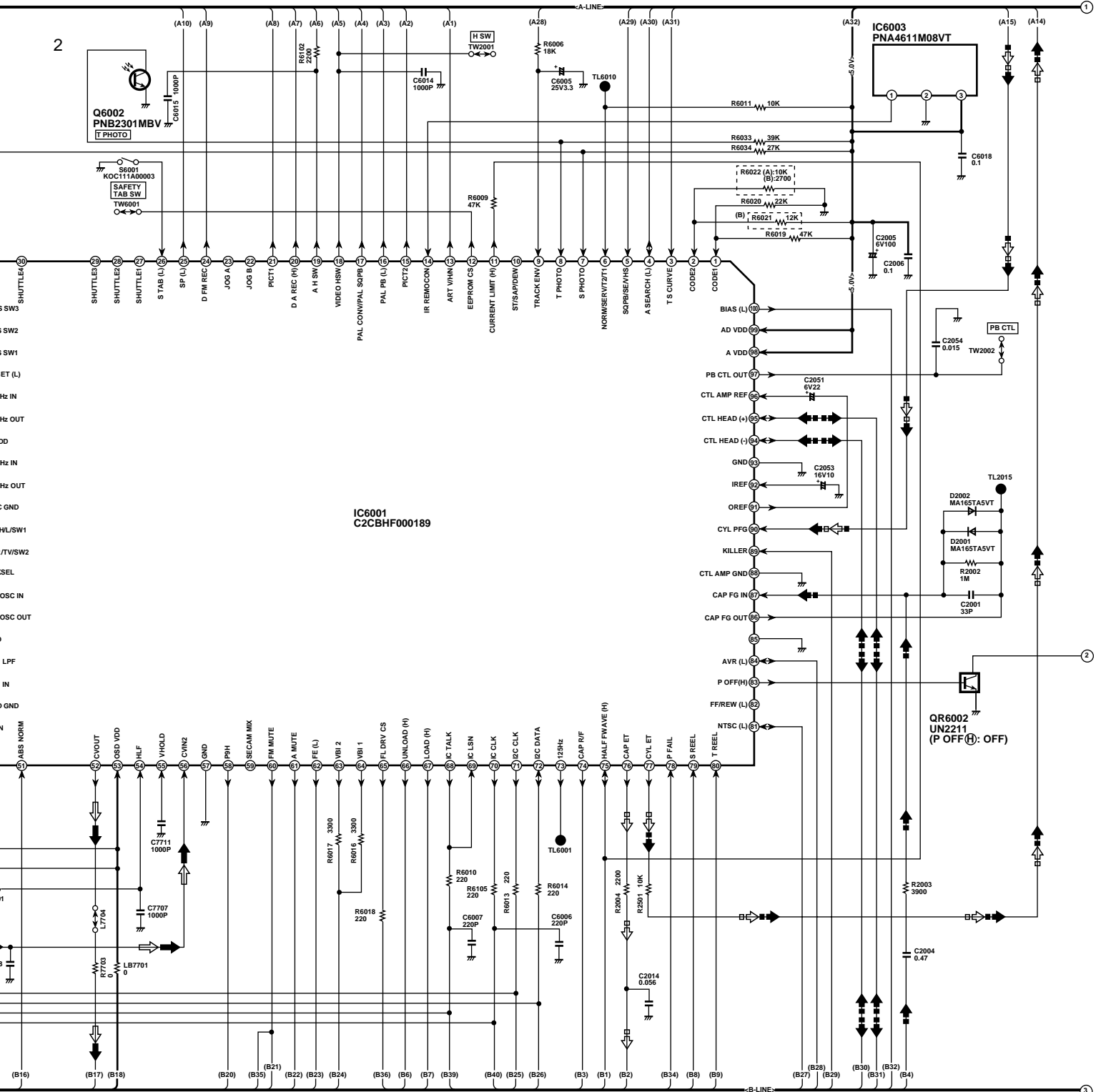
NOTE2: THE DC VOLTAGE INDICATED IN PRIMARY SIDE IS SHOWN THE VOLTAGE WHEN INPUT AC IS 220V.

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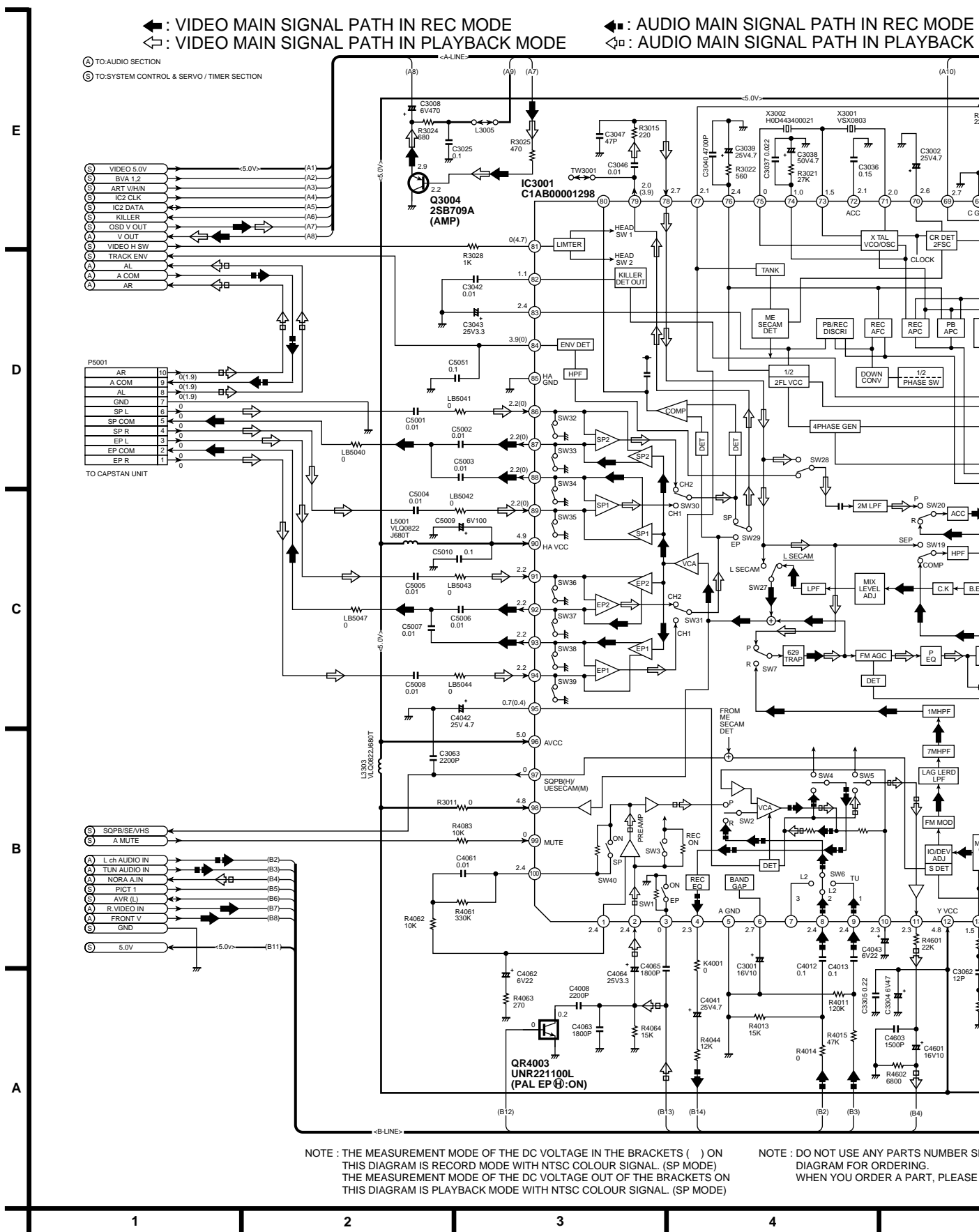


◀ :VIDEO MAIN SIGNAL PATH IN PLAYBACK MODE ◀ ◻ :CAPSTAN SERVO PHASE LOOP ◀ ◻ :CYLINDER SERVO SPEED LOOP
 ◀ ◻ :VIDEO MAIN SIGNAL PATH IN REC MODE ◀ ◻ :CAPSTAN SERVO SPEED LOOP ◀ ◻ :CYLINDER SERVO PHASE LOOP



NV-FJ620A, NV-FJ620EA
 SYSTEM CONTROL & SERVO/TIMER IN MAIN SCHEMATIC DIAGRAM

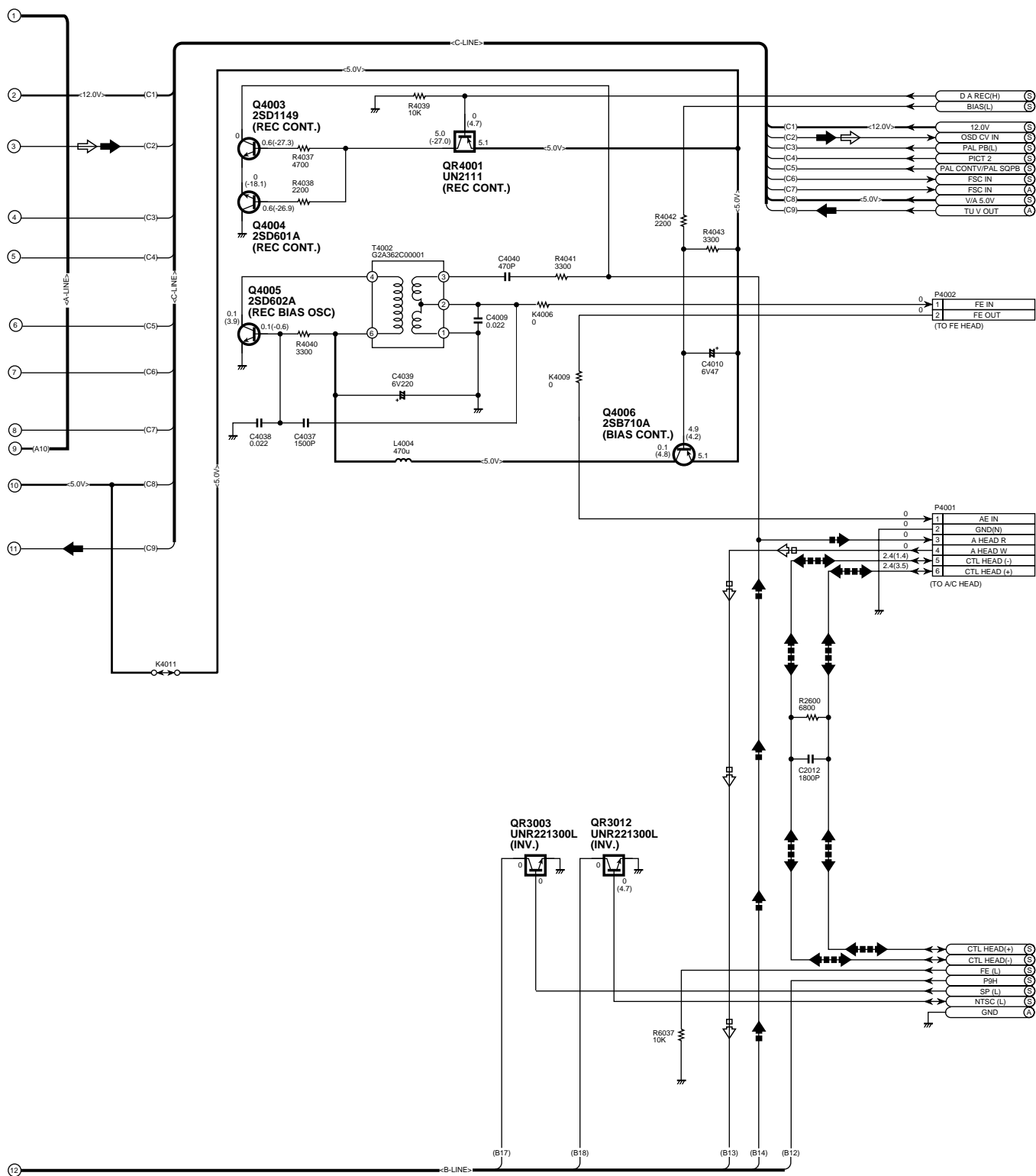




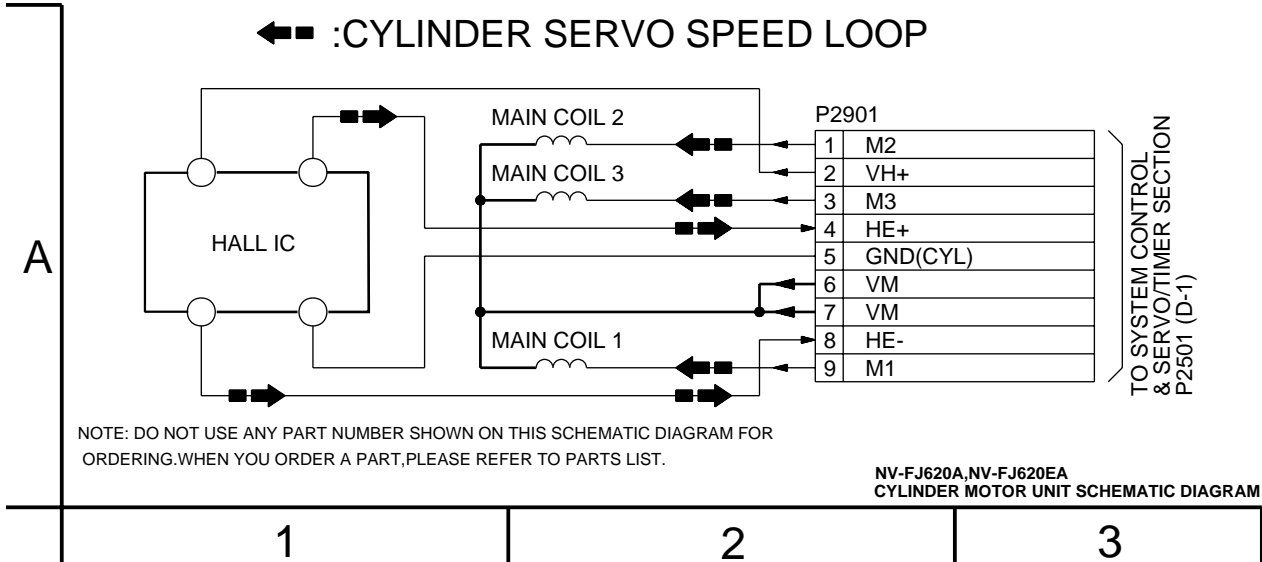


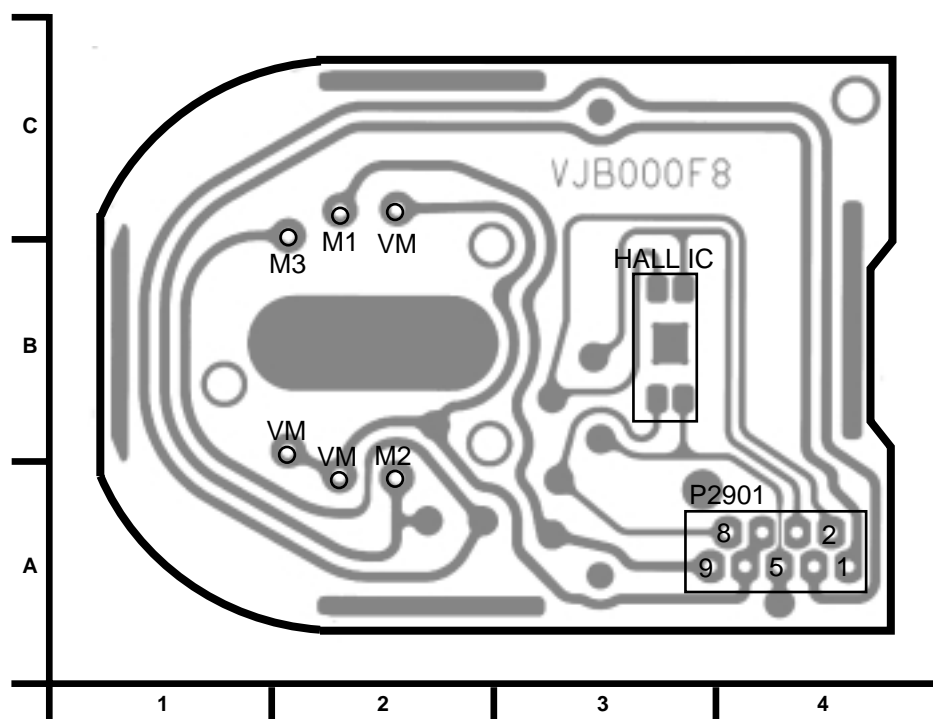
NV-FJ620A, NV-FJ620EA
VIDEO SECTION IN MAIN SCHEMATIC DIAGRAM

9



NV-FJ620A, NV-FJ620EA
VIDEO SECTION IN MAIN SCHEMATIC DIAGRAM

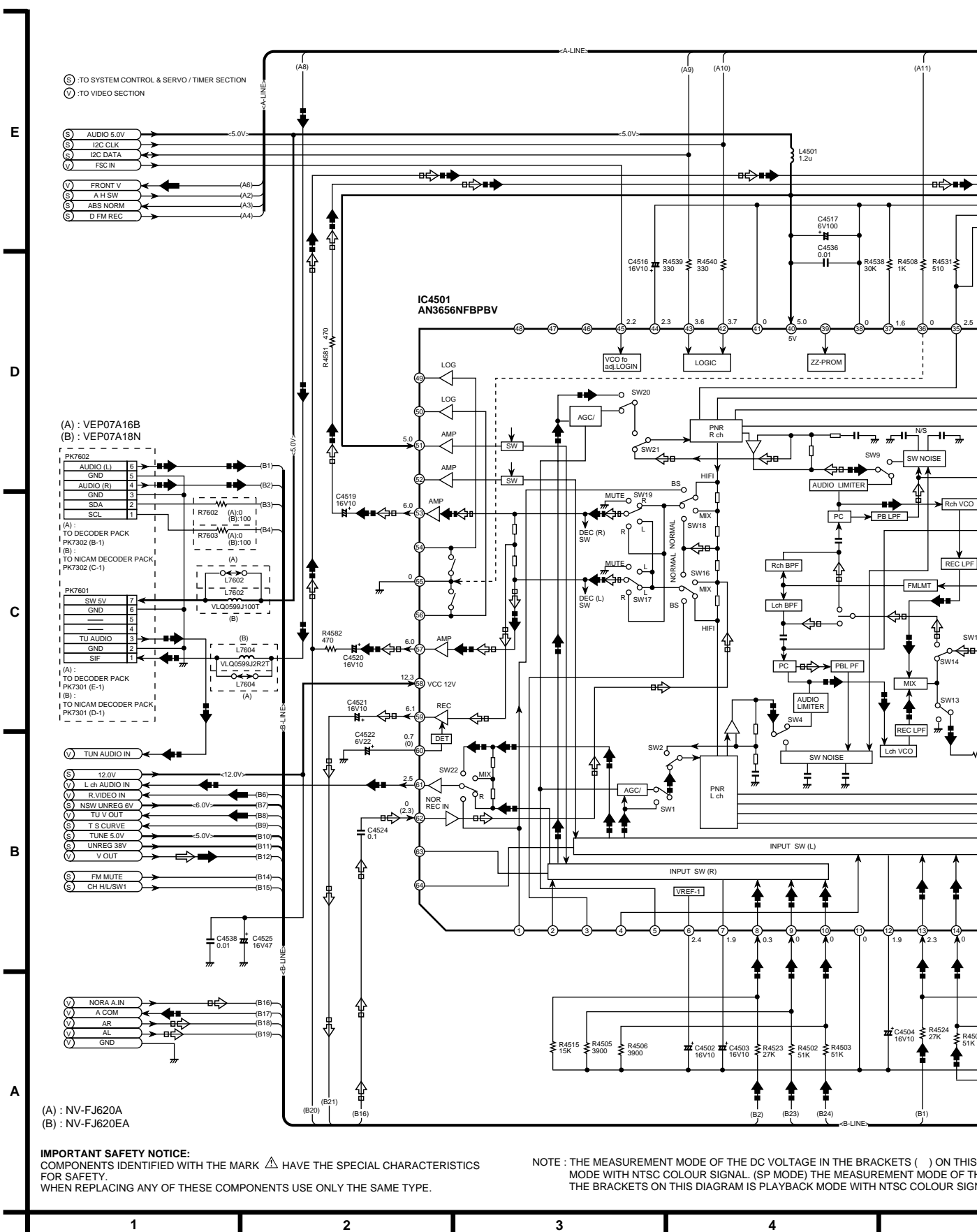




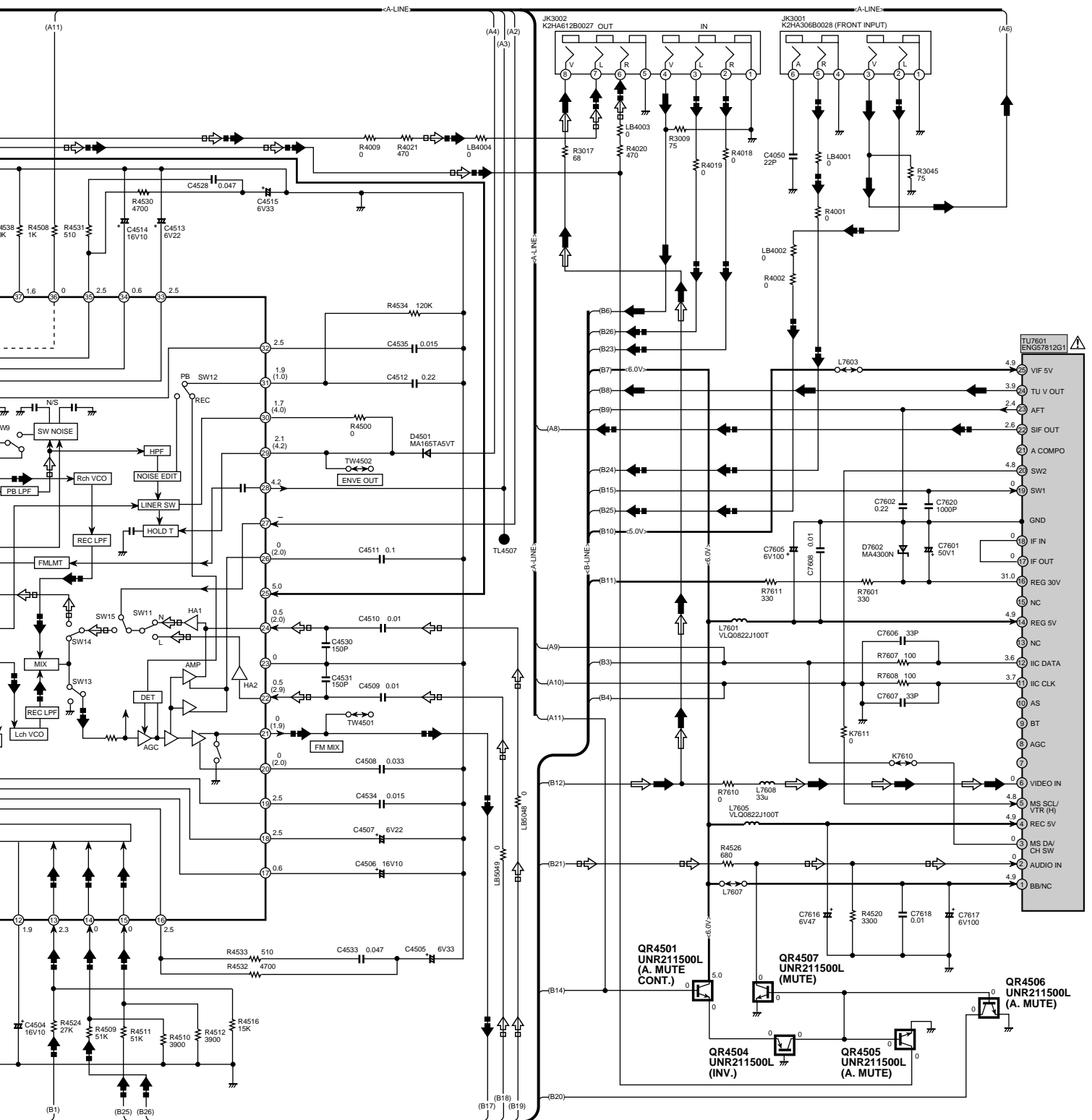
CYLINDER MOTOR UNIT	
Integrated Circuit	
HALL IC	B-3
Connector	
P2901	A-4

ADDRESS INFORMATION

NV-FJ620A,NV-FJ620EA
CYLINDER MOTOR C.B.A
VEP000F8A



◀: VIDEO MAIN SIGNAL PATH IN REC MODE ◀◀: VIDEO MAIN SIGNAL PATH IN PLAYBACK MODE
 ◀◀◀: AUDIO MAIN SIGNAL PATH IN REC MODE ◀◀◀◀: AUDIO MAIN SIGNAL PATH IN PLAYBACK MODE



PACKETS () ON THIS DIAGRAM IS RECORD
 REMENT MODE OF THE DC VOLTAGE OUT OF
 H NTSC COLOUR SIGNAL. (SP MODE)

NOTE : DO NOT USE ANY PARTS NUMBER SHOWN ON THIS SCHEMATIC
 DIAGRAM FOR ORDERING.
 WHEN YOU ORDER A PART, PLEASE REFER TO PARTS LIST.

NV-FJ620A, NV-FJ620EA
 AUDIO SECTION IN MAIN SCHEMATIC DIAGRAM

5

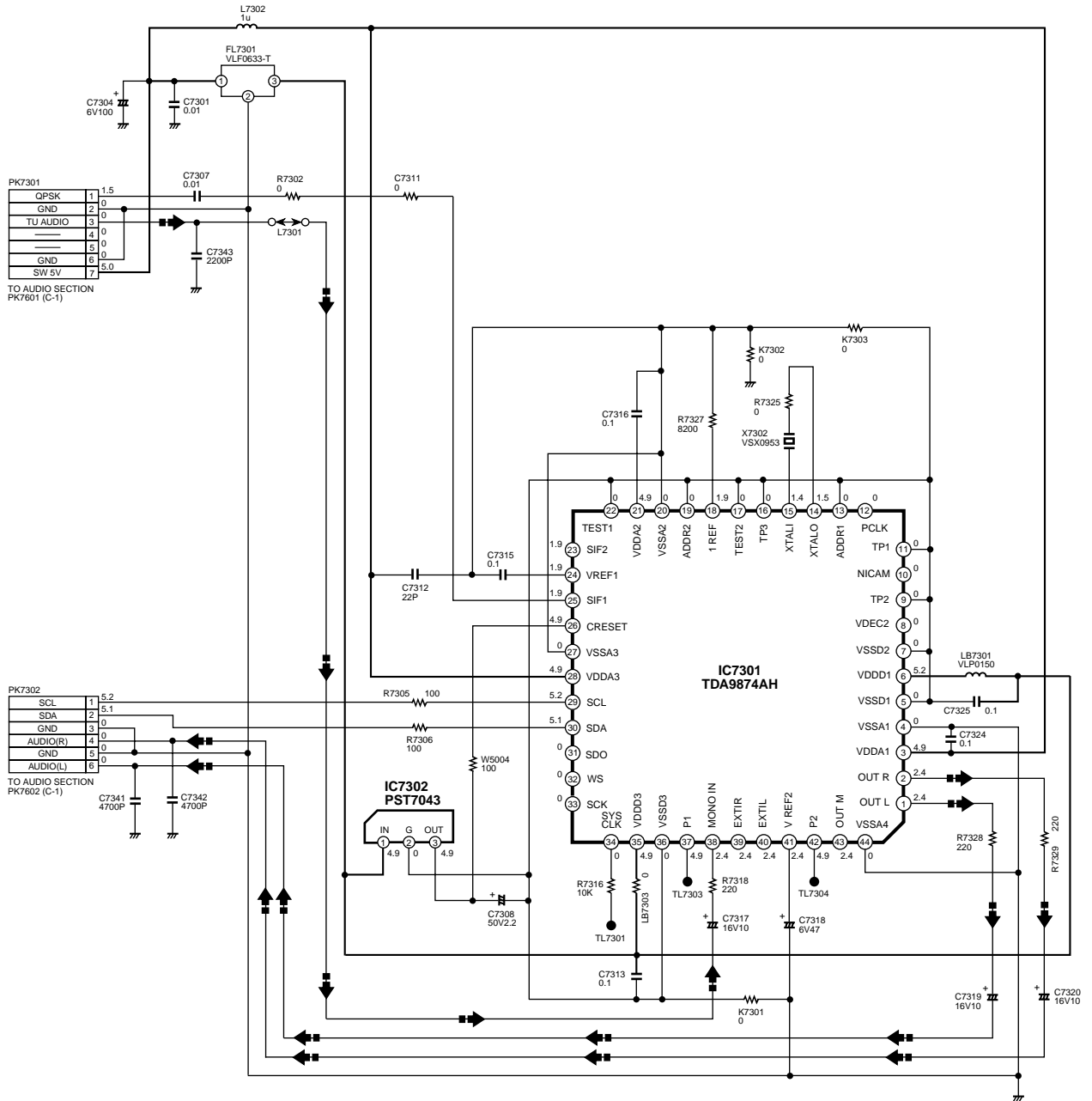
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←:AUDIO SIGNAL PATH



NV-FJ620EA
NICAM DECODER PACK SCHEMATIC DIAGRAM